This listing of claims will replace all prior versions, and listings, of claims in the application

LISTING OF CLAIMS

1. (currently amended) A data storage device in a single integrated circuit unit, comprising:

memory cells having stored data with selectable output start addresses;

said data storage device in a single integrated circuit unit comprising input and output terminals;

wherein said storage device responds to a single data output request provided to said input of said single integrated circuit by outputting, via an internal through connection of said integrated circuit configured to adaptively connect bits of said memory cells to the output terminals, said stored data from said output terminals of said single integrated circuit beginning with a selected output start address that is one of said selectable output start addresses; and

wherein said selectable output start addresses of said memory cells are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request.

2. (currently amended) A data storage device according to claim 1, wherein said selected output start address is determined utilizing address data applied to said input of said data storage device.

3. (previously presented) A data storage device according to claim 2, wherein:

said selected output start address is determined by further utilizing adaptation data applied to said data storage device and;

said adaptation data is related both to said output start address to be employed and an address that is defined by said address data.

4. (currently amended) A data storage device according to claim 3, further comprising:

~~output terminals; and~~

~~an interface provided between memory cells of said data storage device and said output terminals;~~

a control mechanism of an interface at which ~~wherein~~ said adaptation data are used to control said interface.

5. (previously presented) A data storage device according to claim 4, wherein said interface comprises a multiplexer that is driven based on the adaptation data.

6. (previously presented) A data storage device according to claim 4, wherein data stored with an output start address selected from the group consisting of a first output start address and a second output start address are through-connected.

7. (previously presented) A data storage device according to claim 6, wherein said first output start address is an address that is represented by said address data applied to said data storage device.

8. (currently amended) A data storage device, comprising:

memory cells having stored data with selectable output start addresses;

wherein said storage device responds to a data output request by outputting said stored data beginning with a selected output start address;

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request;

wherein said selected output start address is determined utilizing address data applied to said data storage device;

wherein said selected output start address is determined by further utilizing adaptation data applied to said data storage device;

wherein said adaptation data is related both to said output start address to be employed and an address that is defined by said address data;

the data storage device further comprising:

output terminals; and

an interface provided between memory cells of said data storage device and said output terminals;

wherein said adaptation data are used to control said interface;

wherein data stored with an output start address selected from the group consisting of a first output start address and a second output start address are through-connected; and

wherein said second output start address is related to, but different from, said first output start address by a scope defined by a wiring of a multiplexer.

9. (currently amended) A method for outputting data from a data storage device in a single integrated circuit unit, comprising the steps of:

receiving a single data output request by said data storage device provided to said input of said single integrated circuit; and

outputting stored data, via an internal through connection of said integrated circuit configured to adaptively connect bits of the memory cells to said output terminals, from said output terminals of said single integrated circuit, in a quantity of data that is greater than a quantity of data that can be stored between neighboring output start addresses of said memory cells, and beginning said outputting of stored data with a selected output start address which is one of said output start addresses.

10. (previously presented) The method according to claim 9, further comprises the steps of:

applying address data to said data storage device; and

determining said selected output start address by utilizing said address data.

11. (previously presented) The method according to claim 10, further comprising the step of:

defining adaption data as an indicia related to said address data and said output start address;

applying said adaption data to said data storage device, wherein said step of determining said selected output start address utilizes said adaption data.

12. (currently amended) The method according to claim 11, further comprising the step of:

controlling, with said adaption data, said internal through connection ~~an interface~~ provided between memory cells of said data storage device and said output terminals of said data storage device.

13. (previously presented) The method according to claim 12, further comprising the steps of:

controlling a multiplexer contained within said interface by applying said adaption data; and

through-connecting, via said multiplexer, data stored within said data storage device beginning with an address selected from the group consisting of a first output start address and a second output start address.

14. (previously presented) The method according to claim 13, further comprising the step of calculating said first output start address from said address data applied to said data storage device.

15. (previously presented) A method for outputting data from a data storage device, comprising the steps of:

receiving a data output request by said data storage device;

outputting stored data in a quantity of data that is greater than a quantity of data that can be stored between neighboring output start addresses, and beginning said outputting of stored data with a selected output start address which is one of said output start addresses;

applying address data to said data storage device;

determining said selected output start address by utilizing said address data;

defining adaption data as an indicia related to said address data and said output start address;

applying said adaption data to said data storage device, wherein said step of determining said selected output start address utilizes said adaption data;

controlling, with said adaption data, an interface provided between memory cells of said data storage device and output terminals of said data storage device;

controlling a multiplexer contained within said interface by applying said adaption data;

through-connecting, via said multiplexer, data stored within said data storage device beginning with an address selected from the group consisting of a first output start address and a second output start address; and

wiring said multiplexer so that said second output start address is related to, but different from, said first output start address by a scope defined by said wiring.

16. (currently amended) A data storage device in a single integrated circuit unit, comprising:

memory cells having stored data with selectable output start addresses;

said data storage device in a single integrated circuit unit comprising input and output terminals;

wherein said storage device responds to a single data output request provided to said input of said single integrated circuit by outputting, via an internal through connection of said integrated circuit, said stored data from said output terminals of said single integrated circuit beginning with a selected output start address that is one of said selectable output start addresses; and

wherein selectable output start addresses are spaced from one another such that an amount of data that can be stored between neighboring output start addresses is smaller than an amount of data output in response to said data output request; and

wherein the device is selected from the group consisting of a RAM, a ROM, EPROM and flash EPROM.

17. (canceled).

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